

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

WHAT WE CLAIM ARE:

1. A semiconductor device comprising:

a plurality of pixels disposed over a semiconductor substrate in a matrix shape;

5 wherein:

each of the pixels comprises a photodiode, a reset transistor, a source follower transistor and a select transistor;

the photodiode comprises an impurity diffusion region of a first conductivity type and an impurity diffusion region of a second conductivity type
10 stacked in a thickness direction;

each of the reset transistor, the source follower transistor and the select transistor comprises a pair of impurity diffusion regions of the first conductivity type formed in a surface layer of the semiconductor substrate and having a channel region between the impurity diffusion regions and a gate
15 electrode formed over the channel region;

the photodiode, the reset transistor, the source follower transistor and the select transistor are disposed in one active region;

the active region comprises a first area in which the photodiode is disposed and a second area having a first end continuous with the first area and
20 including an area elongated along a first direction; and

each of gate electrodes of the reset transistor, the source follower transistor and the select transistor crosses the area, elongated along the first direction, of the second area, and a cross area between the gate electrode of the reset transistor and the second region, a cross area between the gate electrode
25 of the source follower transistor and the second region and a cross area between

the gate electrode of the select transistor and the second region, are disposed in this order in a direction of departing from the first end,

an intra-pixel wiring line for interconnecting the impurity diffusion region of the reset transistor on the first end side and the gate electrode of the
5 source follower transistor of the pixel;

a reset voltage supply line connected to the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor and being applied with a reset voltage for applying an initial reverse bias to the photodiode;

10 a reset signal line for applying a reset signal to the gate electrode of the reset transistor;

a select signal line disposed for each row of the pixels, the select signal line applying a select signal to the gate electrodes of the select transistors of the pixels in a corresponding row; and

15 a signal read line disposed for each column of the pixels and connected to the impurity diffusion regions, on a side opposite to the first end, of the select transistors of the pixels in a corresponding column.

2. A semiconductor device according to claim 1, wherein:

20 each of the pixels further comprises a transfer transistor disposed in the second area and having a pair of impurity diffusion regions having a channel region formed between the impurity diffusion regions and a gate electrode formed over the channel region;

the gate electrode of the transfer transistor crosses the area,
25 elongated in the first direction, of the second area in an area nearer to the first

end than the cross area between the gate electrode of the reset transistor and the second area, and the impurity diffusion region of the transfer transistor on the first end side is connected to the impurity diffusion region of the first conductivity type of the photodiode; and

5 the semiconductor device further comprises a transfer signal line for applying a transfer signal to the gate electrode of the transfer transistor.

3. A semiconductor device according to claim 2, wherein the transfer signal line is disposed in a same conductive layer as the gate electrode of the transfer
10 transistor.

4. A semiconductor device according to claim 1, wherein the reset signal line is disposed in a same conductive layer as the gate electrode of the reset transistor.

15 5. A semiconductor device according to claim 1, wherein the select signal line is disposed in a same conductive layer as the gate electrode of the select transistor.

6. A semiconductor device according to claim 1, wherein at least a partial region of the intra-pixel wiring line connecting the impurity diffusion region of the reset
20 transistor on the first end side is made of silicon.

7. A semiconductor device according to claim 1, further comprising:
 upper gate protective films covering an upper surface of the gate electrodes of the reset transistor, the source follower transistor and the select
25 transistor;

side gate protective films covering sidewalls of the gate electrodes of the reset transistor, the source follower transistor and the select transistor;

an interlayer insulating film formed over the semiconductor substrate and covering the reset transistor, the source follower transistor and the
5 select transistor;

a first via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region of the reset transistor on the first end side appearing on a bottom of the first via hole;

a second via hole formed through the interlayer insulating film, an
10 upper surface of the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor appearing on a bottom of the second via hole; and

a third via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region of the select transistor on a side
15 opposite to the first end side appearing on a bottom of the third via hole,

wherein:

the intra-pixel wiring line is connected to the impurity diffusion region of the reset transistor on the first end side via the first via hole;

the reset voltage supply line is connected to the impurity diffusion
20 region between the gate electrodes of the reset transistor and the source follower transistor via the second via hole; and

the signal read line is connected to the impurity diffusion region of the select transistor on a side opposite to the first end via the third via hole, and

wherein:

25 the side gate protective film covering the sidewall of the gate

electrode of the reset transistor appearing on a side of the first via hole;

the side gate protective film covering the sidewall of the gate electrode of the reset transistor and the side gate protective film covering the sidewall of the source follower transistor appearing on a side of the second via

5 hole; or

the side gate protective film covering the sidewall of the select transistor appearing on a side of the third via hole.

8. A semiconductor device according to claim 7, wherein the interlayer
10 insulating film comprises a layer covering an area of the upper gate protective films and the side gate protective films not appearing on the sides of the first to third via holes, the layer being made of material having etching characteristics different from the upper gate protective films and the side gate protective films.

15 9. A semiconductor device according to claim 7, wherein:

each of the pixels further comprises a transfer transistor disposed in the second area and having a pair of impurity diffusion regions having a channel region formed between the impurity diffusion regions and a gate electrode formed over the channel region;

20 the gate electrode of the transfer transistor crosses the area, elongated in the first direction, of the second area in an area nearer to the first end than the cross area between the gate electrode of the reset transistor and the second area, and the impurity diffusion region of the transfer transistor on the first end side is connected to the impurity diffusion region of the first conductivity
25 type of the photodiode; and

the semiconductor device further comprises:

a transfer signal line for applying a transfer signal to the gate electrode of the transfer transistor;

an upper gate protective film covering an upper surface of the gate electrode of the transfer transistor; and

a side gate protective film covering sidewalls of the gate electrode of the transfer transistor,

wherein the side gate protective film covering the sidewalls of the gate electrode of the transfer transistor appearing on a side of the first via hole.

10

10. A semiconductor device according to claim 1, further comprising:

an interlayer insulating film formed over the semiconductor substrate and covering the reset transistor, the source follower transistor and the select transistor;

15 a first via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region of the reset transistor on the first end side appearing on a bottom of the first via hole;

a second via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor appearing on a bottom of the

20 second via hole;

a third via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region of the select transistor on a side opposite to the first end side appearing on a bottom of the third via hole; and

25 a sidewall spacer made of insulating material and covering a side of

each of the first to third via holes,

wherein:

the intra-pixel wiring line is connected to the impurity diffusion region of the reset transistor on the first end side via the first via hole;

5 the reset voltage supply line is connected to the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor via the second via hole; and

the signal read line is connected to the impurity diffusion region of the select transistor on a side opposite to the first end side via the third via hole.

10

11. A semiconductor device according to claim 10, wherein a sidewall of the gate electrode of the reset transistor appears on a side of the first via hole, sidewalls of the gate electrodes of the reset transistor and the source follower transistor appear on a sidewall of the second via hole, and a sidewall of the gate
15 electrode of the select transistor appears on a sidewall of the third via hole.

12. A semiconductor device according to claim 10, wherein:

each of the pixels further comprises a transfer transistor disposed in the second area and having a pair of impurity diffusion regions having a
20 channel region formed between the impurity diffusion regions and a gate electrode formed over the channel region; and

a transfer signal line for applying a transfer signal to the gate electrode of the transfer transistor,

wherein:

25 the gate electrode of the transfer transistor crosses the area,

elongated in the first direction, of the second area in an area nearer to the first end than the cross area between the gate electrode of the reset transistor and the second area, and the impurity diffusion region of the transfer transistor on the first end side is connected to the impurity diffusion region of the first conductivity

5 type of the photodiode; and

a sidewall of the gate electrode of the transfer transistor appears on a sidewall of the first via hole.

13. A semiconductor device according to claim 1, wherein the intra-pixel wiring
10 line from a region connected to the impurity diffusion region of the reset transistor on the first end side to a region connected to the gate electrode of the source follower transistor comprises a silicon layer or a lamination layer including a silicon layer as a lowest layer.

15 14. A semiconductor device according to claim 13, wherein one of the reset signal line and the select signal line is disposed in a same conductive layer as the intra-pixel wiring line.

15. A semiconductor device according to claim 2, wherein the intra-pixel wiring
20 line from a region connected to the impurity diffusion region of the reset transistor on the first end side to a region connected to the gate electrode of the source follower transistor comprises a silicon layer or a lamination layer including a silicon layer as a lowest layer.

25 16. A semiconductor device according to claim 15, wherein one of the reset

signal line, the select signal line and the transfer signal line is disposed in a same conductive layer as the intra-pixel wiring line.

17. A semiconductor device according to claim 1, wherein the first area
5 comprises a straight outer periphery and the area, elongated along the first direction, of the second area runs in parallel to the straight outer periphery of the first area.
18. A semiconductor device comprising:
10 a plurality of pixels disposed over a semiconductor substrate in a matrix shape;
wherein:
each of the pixels comprises a photodiode, a reset transistor; a source follower transistor and a select transistor;
15 the photodiode comprises an impurity diffusion region of a first conductivity type and an impurity diffusion region of a second conductivity type stacked in a thickness direction;
each of the reset transistor, the source follower transistor and the select transistor comprises a pair of impurity diffusion regions of a first
20 conductivity type formed in a surface layer of the semiconductor substrate and having a channel region between the impurity diffusion regions and a gate electrode formed over the channel region;
the photodiode, the reset transistor, the source follower transistor and the select transistor are disposed in one active region;
25 the active region comprises a first area in which the photodiode is

disposed and a second area having a first end continuous with the first area an elongated shape; and

each of gate electrodes of the reset transistor, the source follower transistor and the select transistor crosses the second area, and a cross area

5 between the gate electrode of the reset transistor and the second region, a cross area between the gate electrode of the source follower transistor and the second region and a cross area between the gate electrode of the select transistor and the second region, are disposed in this order in a direction of departing from the first end,

10 an intra-pixel wiring line for interconnecting the impurity diffusion region of the reset transistor on the first end side and the gate electrode of the source follower transistor of the pixel, at least a region of the intra-pixel wiring line connected to the impurity diffusion region of the reset transistor on the first end side being made of silicon;

15 a reset voltage supply line connected to the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor and being applied with a reset voltage for applying an initial reverse bias to the photodiode;

a reset signal line for applying a reset signal to the gate electrode of
20 the reset transistor;

a select signal line disposed for each row of the pixels, the select signal line applying a select signal to the gate electrodes of the select transistors of the pixels in a corresponding row; and

a signal read line disposed for each column of the pixels and
25 connected to the impurity diffusion regions, on a side opposite to the first end, of

the select transistors of the pixels in a corresponding column.

19. A semiconductor device according to claim 18, wherein:

each of the pixels further comprises a transfer transistor disposed
5 in the second area and having a pair of impurity diffusion regions having a
channel region formed between the impurity diffusion regions and a gate
electrode formed over the channel region;

the gate electrode of the transfer transistor crosses the second
area between the gate electrode of the reset transistor and the first end of the
10 second area, and the impurity diffusion region of the transfer transistor on the first
end side is connected to the impurity diffusion region of the first conductivity type
of the photodiode; and

the semiconductor device further comprises a transfer signal line
for applying a transfer signal to the gate electrode of the transfer transistor.

15

20. A semiconductor device according to claim 18, wherein the intra-pixel wiring
line from a region connected to the impurity diffusion region of the reset transistor
on the first end side to a region connected to the gate electrode of the source
follower transistor of the pixel comprises a silicon layer or a lamination layer
20 including a silicon layer as a lowest layer.

21. A semiconductor device according to claim 20, wherein one of the reset
signal line and the select signal line is disposed in a same conductive layer as the
intra-pixel wiring line.

25

22. A semiconductor device comprising:

a plurality of pixels disposed over a semiconductor substrate in a matrix shape;

wherein:

5 each of the pixels comprises a photodiode, a reset transistor; a source follower transistor and a select transistor;

the photodiode comprises an impurity diffusion region of a first conductivity type and an impurity diffusion region of a second conductivity type stacked in a thickness direction;

10 each of the reset transistor, the source follower transistor and the select transistor comprises a pair of impurity diffusion regions of the first conductivity type formed in a surface layer of the semiconductor substrate and having a channel region between the impurity diffusion regions and a gate electrode formed over the channel region;

15 the photodiode, the reset transistor, the source follower transistor and the select transistor are disposed in one active region;

the active region comprises a first area in which the photodiode is disposed and a second area having a first end continuous with the first area and an elongated shape; and

20 each of gate electrodes of the reset transistor, the source follower transistor and the select transistor crosses the second area, and a cross area between the gate electrode of the reset transistor and the second area, a cross area between the gate electrode of the source follower transistor and the second area and a cross area between the gate electrode of the select transistor and the
25 second area, are disposed in this order in a direction of departing from the first

end,

an intra-pixel wiring line for interconnecting the impurity diffusion region of the reset transistor on the first end side and the gate electrode of the source follower transistor of the pixel;

5 a reset voltage supply line connected to the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor and being applied with a reset voltage for applying an initial reverse bias to the photodiode;

a reset signal line for applying a reset signal to the gate electrode of
10 the reset transistor;

a select signal line disposed for each row of the pixels, the select signal line applying a select signal to the gate electrodes of the select transistors of the pixels in a corresponding row;

a signal read line disposed for each column of the pixels and
15 connected to the impurity diffusion regions, on a side opposite to the first end, of the select transistors of the pixels in a corresponding column;

an upper gate protective film covering an upper surface of the gate electrodes of the reset transistor, the source follower transistor and the select transistor;

20 a side gate protective film covering sidewalls of the gate electrodes of the reset transistor, the source follower transistor and the select transistor;

an interlayer insulating film formed over the semiconductor substrate and covering the reset transistor, the source follower transistor and the select transistor;

25 a first via hole formed through the interlayer insulating film, an

upper surface of the impurity diffusion region of the reset transistor on the first end side appearing on a bottom of the first via hole, and the side gate protective film covering the sidewall of the gate electrode of the reset transistor appearing on a sidewall of the first via hole;

5 a second via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor appearing on a bottom of the second via hole, and the side gate protective film covering the sidewall of the gate electrode of the reset transistor and the side gate protective film covering
10 the sidewall of the source follower transistor appearing on a sidewall of the second via hole; and

 a third via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region of the select transistor on a side opposite to the first end side appearing on a bottom of the third via hole, and the
15 side gate protective film covering the sidewall of the gate electrode of the select transistor appearing on a sidewall of the third via hole,

 wherein:

 the intra-pixel wiring line is connected to the impurity diffusion region of the reset transistor on the first end side via the first via hole;

20 the reset voltage supply line is connected to the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor via the second via hole; and

 the signal read line is connected to the impurity diffusion region of the select transistor on a side opposite to the first end side via the third via hole.

25

23. A semiconductor device according to claim 22, wherein the interlayer insulating film comprises a layer covering an area of the upper gate protective films and the side gate protective films not appearing on the sidewalls of the first to third via holes, the layer being made of material having etching characteristics
5 different from the upper gate protective films and the side gate protective films.

24. A semiconductor device comprising:

a plurality of pixels disposed over a semiconductor substrate in a matrix shape;

10 wherein:

each of the pixels comprises a photodiode, a reset transistor; a source follower transistor and a select transistor;

the photodiode comprises an impurity diffusion region of a first conductivity type and an impurity diffusion region of a second conductivity type
15 stacked in a thickness direction;

each of the reset transistor, the source follower transistor and the select transistor comprises a pair of impurity diffusion regions of the first conductivity type formed in a surface layer of the semiconductor substrate and having a channel region between the impurity diffusion regions and a gate
20 electrode formed over the channel region;

the photodiode, the reset transistor, the source follower transistor and the select transistor are disposed in one active region;

the active region comprises a first area in which the photodiode is disposed and a second area having a first end continuous with the first area and
25 an elongated shape; and

each of gate electrodes of the reset transistor, the source follower transistor and the select transistor crosses the second area, and a cross area between the gate electrode of the reset transistor and the second area, a cross area between the gate electrode of the source follower transistor and the second area and a cross area between the gate electrode of the select transistor and the second area, are disposed in this order along a direction of departing from the first end,

an intra-pixel wiring line for interconnecting the impurity diffusion region of the reset transistor on the first end side and the gate electrode of the source follower transistor of the pixel;

a reset voltage supply line connected to the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor and being applied with a reset voltage for applying an initial reverse bias to the photodiode;

a reset signal line for applying a reset signal to the gate electrode of the reset transistor;

a select signal line disposed for each row of the pixels, the select signal line applying a select signal to the gate electrodes of the select transistors of the pixels in a corresponding row;

a signal read line disposed for each column of the pixels and connected to the impurity diffusion regions, on a side opposite to the first end, of the select transistors of the pixels in a corresponding column;

an interlayer insulating film formed over the semiconductor substrate and covering the reset transistor, the source follower transistor and the select transistor;

a first via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region of the reset transistor on the first end side appearing on a bottom of the first via hole;

a second via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor appearing on a bottom of the second via hole;

a third via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region of the select transistor on a side opposite to the first end side appearing on a bottom of the third via hole; and

a sidewall spacer made of insulating material and covering a sidewall of each of the first to third via holes,

wherein:

the intra-pixel wiring line is connected to the impurity diffusion region of the reset transistor on the first end side via the first via hole;

the reset voltage supply line is connected to the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor via the second via hole; and

the signal read line is connected to the impurity diffusion region of the select transistor on a side opposite to the first end via the third via hole.

25. A semiconductor device according to claim 24, wherein a sidewall of the gate electrode of the reset transistor appears on a sidewall of the first via hole, sidewalls of the gate electrodes of the reset transistor and the source follower transistor appear on a sidewall of the second via hole, and a sidewall of the gate

electrode of the select transistor appears on a sidewall of the third via hole.

26. A semiconductor device comprising:

5 a plurality of pixels disposed over a semiconductor substrate in a matrix shape;

wherein:

each of the pixels comprises a photodiode, a reset transistor, a source follower transistor and a select transistor;

10 the photodiode comprises an impurity diffusion region of a first conductivity type and an impurity diffusion region of a second conductivity type stacked in a thickness direction;

each of the reset transistor, the source follower transistor and the select transistor comprises a pair of impurity diffusion regions of the first conductivity type formed in a surface layer of the semiconductor substrate and
15 having a channel region between the impurity diffusion regions and a gate electrode formed over the channel region;

the photodiode, the reset transistor, the source follower transistor and the select transistor are disposed in one active region;

20 the active region comprises a first area in which the photodiode is disposed and a second area having a first end continuous with the first area and including an area elongated along a first direction; and

each of gate electrodes of the reset transistor, the source follower transistor and the select transistor crosses the area, elongated along the first direction, of the second area, and a cross area between the gate electrode of the
25 reset transistor and the second region, a cross area between the gate electrode

of the source follower transistor and the second region and a cross area between the gate electrode of the select transistor and the second region, are disposed in this order in a direction of departing from the first end,

an intra-pixel wiring line for interconnecting the impurity diffusion
5 region of the reset transistor on the first end side and the gate electrode of the source follower transistor of the pixel;

a reset voltage supply line connected to the impurity diffusion
region between the gate electrodes of the reset transistor and the source follower
transistor and being applied with a reset voltage for applying an initial reverse
10 bias to the photodiode;

a reset signal line for applying a reset signal to the gate electrode of
the reset transistor;

a select signal line disposed for each row of the pixels, the select
signal line applying a select signal to the gate electrodes of the select transistors
15 of the pixels in a corresponding row;

a signal read line disposed for each column of the pixels and
connected to the impurity diffusion regions, on a side opposite to the first end, of
the select transistors of the pixels in a corresponding column;

upper gate protective films covering an upper surface of the gate
20 electrodes of the reset transistor, the source follower transistor and the select
transistor;

side gate protective films covering sidewalls of the gate electrodes
of the reset transistor, the source follower transistor and the select transistor;

an interlayer insulating film formed over the semiconductor
25 substrate and covering the reset transistor, the source follower transistor and the

select transistor;

a first via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region of the reset transistor on the first end side appearing on a bottom of the first via hole;

5 a second via hole formed through the interlayer insulating film, an upper surface of the impurity diffusion region between the gate electrodes of the reset transistor and the source follower transistor appearing on a bottom of the second via hole; and

a third via hole formed through the interlayer insulating film, an
10 upper surface of the impurity diffusion region of the select transistor on a side opposite to the first end side appearing on a bottom of the third via hole,

wherein each of the first via hole, the second via hole and the third via hole has self-aligned contact structure.

15